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Circuit Decompositions of Eulerian Graphs

Genghua Fan[1]

Department of Mathematics, Arizona State University, Tempe, Arizona 85287

and

Cun-Quan Zhang[2]

Department of Mathematics, West Virginia University, Morgantown, West Virginia 26506-6310

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Let G be an eulerian graph. For each vertex $v \in V(G)$, let $P(v)$ be a partition of the edges incident with v and set $\mathscr{P} = \bigcup_{v \in V(G)} P(v)$, called a forbidden system of G. We say that $\mathscr{P}$ is admissible if $|P \cap T| \leqslant \frac{1}{2}|T|$ for every $P \in \mathscr{P}$ and every edge cut T of G. H. Fleischner and A. Frank (1990, *J. Combin. Theory Ser. B* **50**, 245–253) proved that if G is planar and $\mathscr{P}$ is any admissible forbidden system of G, then G has a circuit decomposition $\mathscr{F}$ such that $|C \cap P| \leqslant 1$ for every $C \in \mathscr{F}$ and every $P \in \mathscr{P}$. We generalize this result to all eulerian graphs that do not contain K_5 as a minor. As a consequence, a conjecture of Sabidussi is settled for graphs that do not contain K_5 as a minor. Also, as a byproduct, our proof provides a different approach to the circuit cover theorem of B. Alspach, L. A. Goddyn, and C.-Q. Zhang (1994, *Trans. Amer. Math. Soc.* **344**, No. 1, 131–154).

Key Words: circuit decomposition; eulerian graph.

1. INTRODUCTION

By a *circuit*, we mean a connected 2-regular graph, while a *cycle* is the union of edge-disjoint circuits. An *eulerian* graph is a connected cycle. Loops and multiple edges are allowed in graphs. Sometimes, we identify a graph with its edge-set. The *symmetric difference* of two cycles A and B, denoted by $A \triangle B$, is the cycle induced by $(E(A) \cup E(B)) \backslash (E(A) \cap E(B))$. Let G be a graph. A *minor* of G is a graph obtained from G by contractions of edges and deletions of vertices and edges. For a vertex $v \in V(G)$, the set of edges of G incident with v is denoted by $E_G(v)$ (if no confusion occurs, we simply write $E(v)$). The *degree* of a vertex v in G, denoted by $d_G(v)$, is the number of edges incident with v in G (if no confusion occurs, we simply

[1] Current address: Institute of System Science, Chinese Academy of Sciences, Beijing 100080, China.

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write $d(v)$). An *edge* (*vertex*) *cut* of G is a minimal set of edges (vertices) whose removal increases the number of components.

Let G be an eulerian graph. For a vertex v in G, a *forbidden set* incident with v, denoted by $\mathscr{P}(v)$, is a partition of $E(v)$ (the set of edges incident with v). A member of $\mathscr{P}(v)$ is called a *forbidden part* (incident with v). The set $\mathscr{P} = \bigcup_{v \in V(G)} \mathscr{P}(v)$ is called a *forbidden system* of G. $\mathscr{P}$ is said to be *admissible* if $|P \cap T| \leqslant \frac{1}{2}|T|$ for every forbidden part $P \in \mathscr{P}$ and every edge cut T of G. If $\mathscr{P}$ is an admissible forbidden system of G, we simply say that $(G, \mathscr{P})$ is *admissible*. A *circuit decomposition* of G is a set of edge-disjoint circuits (of G) whose union is G. We say that $(G, \mathscr{P})$ has a *compatible circuit decomposition* (CCD) if G has a circuit decomposition $\mathscr{F}$ such that $|E(C) \cap P| \leqslant 1$ for every $C \in \mathscr{F}$ and every $P \in \mathscr{P}$. A forbidden part is *trivial* if it consists of a single edge, and *non-trivial* otherwise. A vertex v in $(G, \mathscr{P})$ is *trivial* (with respect to $\mathscr{P}$) if every forbidden part incident with v is trivial, and *non-trivial* otherwise. Clearly, if every vertex of $(G, \mathscr{P})$ is trivial, then any circuit decomposition of G is a CCD of $(G, \mathscr{P})$. Let $\mathscr{F} = \{C_1, C_2, ..., C_m\}$ be a set of cycles of G. $\mathscr{F}$ is called a *compatible cycle decomposition* of $(G, \mathscr{P})$ if $|C_i \cap P| \leqslant 1$ for every C_i, $1 \leqslant i \leqslant m$, and every $P \in \mathscr{P}$. By this definition, if $\mathscr{F}$ is a compatible cycle decomposition of $(G, \mathscr{P})$, then arbitrary circuit decompositions of C_i into circuits, $1 \leqslant i \leqslant m$, result in a CCD of $(G, \mathscr{P})$. Therefore, $(G, \mathscr{P})$ has a CCD if and only if it has a compatible cycle decomposition.

There are close connections between compatible circuit decompositions of eulerian graphs and faithful circuit covers of weighted graphs. Let w be a weight function from the edge-set of a graph G to the set of non-negative integers. For $T \subseteq E(G)$, define $w(T) = \sum_{e \in T} w(e)$. (G, w) is said to be *eulerian* if $w(T)$ is even for every edge cut T of G and is said to be *admissible* if $w(e) \leqslant \frac{1}{2}w(T)$ for every edge cut T and any edge $e \in T$. A family $\mathscr{F}$ of circuits of G is called a *faithful circuit cover* of (G, w) if each edge e of G is contained in exactly $w(e)$ circuits of $\mathscr{F}$.

Let G be an eulerian graph with an admissible forbidden system $\mathscr{P}$. For each vertex v, let $\mathscr{P}(v) = \{P_1, P_2, ..., P_k\}$. We split v into k vertices $v_1, v_2, ..., v_k$ such that v_i is incident with the edges in P_i and then add a new vertex v' joined to each v_i by a new edge of weight $|P_i|$, $1 \leqslant i \leqslant k$. Let H be the new graph obtained by applying this operation to every vertex v of G, and complete the weight function by assigning to every old edge (edge of G) weight 1. If we denote this weight function by w, then $(G, \mathscr{P})$ has a compatible circuit decomposition if and only if (H, w) has a faithful circuit cover.

Conversely, if H is a graph with an admissible, eulerian weight w, let G be the eulerian graph obtained from H by replacing each edge e by a set P_e of $w(e)$ parallel edges (thus deleting e if $w(e) = 0$ and leaving e unaltered if $w(e) = 1$). Consider each P_e as a forbidden part (of G) incident with

either end of e (in H). Then, the set $\mathscr{P}$ of all these forbidden parts is an admissible forbidden system of G. Evidently, (H, w) has a faithful circuit cover if and only if $(G, \mathscr{P})$ has a CCD.

It is clear that admissibility is necessary for $(G, \mathscr{P})$ to have a CCD. But, it is not sufficient. This can be seen from the following example. Let K_5 be the complete graph on five vertices $\{v_i: 0 \leqslant i \leqslant 4\}$. The forbidden set incident with v_i is defined by $\mathscr{P}(v_i) = \{\{v_iv_{i-1}, v_iv_{i+1}\}, \{v_iv_{i-2}, v_iv_{i+2}\}\}$, where $0 \leqslant i \leqslant 4$ and the subscripts are read modulo 5. Set $\mathscr{P} = \bigcup_{i=0}^{i=4} \mathscr{P}(v_i)$. Then $(K_5, \mathscr{P})$ is admissible, but has no CCD. Fleischner and Frank [6] proved that if G is a planar graph with an admissible forbidden system $\mathscr{P}$, then $(G, \mathscr{P})$ has a CCD. This result together with the prior one in [4] simplifies the proofs of Seymour's circuit cover theorem [8] and even circuit decomposition theorem [9] (see [5, 6]). Applications of the compatible circuit decompositions of planar graphs to the Chinese Postman Problem and Shortest Circuit Cover Problem can be found in Fleischner and Guan [7]. It is known that planar graphs do not contain K_5 or $K_{3,3}$ as a minor. The following theorem generalizes Fleischner and Frank's result [6].

THEOREM 1.1. *Let G be an eulerian graph with an admissible forbidden system $\mathscr{P}$. If G does not contain K_5 as a minor, then $(G, \mathscr{P})$ has a compatible circuit decomposition.*

The proof of Theorem 1.1 is divided into two parts (part one, Sections 2, 3, and 4; and part two, Sections 5 and 6). In the first part, we prove that Theorem 1.1 is true for all $(G, \mathscr{P})$ in which each forbidden part has cardinality at most two (Theorem 4.2) (which generalizes an early result (Theorem 3.1) by Fleischner for planar graphs [4]). In the second part, we prove that if Theorem 1.1 is not true, then there would be counterexamples $(G, \mathscr{P})$ in which each forbidden part has cardinality at most 2 (Theorem 6.5). The combination of these two results gives Theorem 1.1.

Let $e_1e_2 \cdots e_m$ be an Euler tour of an eulerian graph G. The forbidden system *induced* by the tour is defined by $\mathscr{P} = \{\{e_i, e_{i+1}\}: 1 \leqslant i \leqslant m$ and $e_{m+1} = e_1\}$. Sabidussi conjectured (see [5]) that if G contains no vertex of degree 2, then $(G, \mathscr{P})$ has a CCD. By Theorem 1.1, Sabidussi's Conjecture is true if G does not contain K_5 as a minor. As another application of Theorem 1.1, Zhang [10] generalizes a result of Seymour [9] by proving that if G is an eulerian graph containing no K_5-minor, and in addition, if each block of G has an even number of edges, then G can be decomposed into circuits of even length. Theorem 1.1 is also applied to prove that every 2-connected graphs containing no K_5-minor has a circular 2-cell embedding in some 2-manifold [11]. Also, as a byproduct (Section 7), our proof provides a different approach to the circuit cover theorem of Alspach, Goddyn, and Zhang [2].

2. MINIMAL CONTRA-PAIRS

DEFINITION 2.1. Let $\mathscr{B}$ denote the set of all admissible pairs $(G, \mathscr{P})$. Define a partial order $\preccurlyeq$ on $\mathscr{B}$ as follows. $(G_1, \mathscr{P}_1) \preccurlyeq (G_2, \mathscr{P}_2)$ if G_1 is a subgraph of G_2 and each member of $\mathscr{P}_1$ is a subset of some member of $\mathscr{P}_2$. If $(G_1, \mathscr{P}_1) \preccurlyeq (G_2, \mathscr{P}_2)$ but $(G_1, \mathscr{P}_1) \neq (G_2, \mathscr{P}_2)$, we write $(G_1, \mathscr{P}_1) \prec (G_2, \mathscr{P}_2)$. A pair $(G, \mathscr{P}) \in \mathscr{B}$ is called a *contra-pair* if it has no compatible circuit decompositions. A *minimal contra-pair* is a contra-pair that is minimal with respect to the partial order $\preccurlyeq$ defined above.

Before the proofs of the main results, we present a few lemmas which will provide some general structures about a minimal contra-pair. Note that the main theorems in this paper are minor-closed results. Thus, we could not apply the vertex splitting method since vertex splitting operations might create some un-expected minors.

DEFINITION 2.2. Let G be an eulerian graph with the maximum degree at most four and T be a vertex cut of G separating G into two parts G_1 and G_2 that $G_1 \cap G_2 = T$ and $G_1 \cup G_2 = G$. A vertex $x \in T$ is called an *even separator* if $d_{G_1}(x) = d_{G_2}(x) = 2$, and *odd separator* otherwise. An even separator x is *balanced* if $\mathscr{P}(x)$ has a forbidden part $\{e, f\}$ such that $e \in E(G_1)$ and $f \in E(G_2)$, and *unbalanced* otherwise.

LEMMA 2.3. *Let G be a 4-regular graph and $\mathscr{P}$ be a forbidden system of G with $|P| \leqslant 2$ for each $P \in \mathscr{P}$. Then $\mathscr{P}$ is admissible in G if and only if no cut-vertex of G is an unbalanced, even separator in $(G, \mathscr{P})$.*

DEFINITION 2.4. Let G be an eulerian graph with the maximum degree at most four and $\mathscr{P}$ be a forbidden system of G with $|P| \leqslant 2$ for each $P \in \mathscr{P}$. Let v be a non-trivial vertex of degree 4 in $(G, \mathscr{P})$ and let $\{e, f\}$ be a forbidden part incident with v. By *splitting* v (with respect to $\mathscr{P}$) we mean that v is split into two vertices, each of degree 2, such that e, f are incident with the same vertex. The *split* of $(G, \mathscr{P})$, denoted by $SP(G, \mathscr{P})$, is the graph obtained from $(G, \mathscr{P})$ by splitting every non-trivial vertex of degree 4.

LEMMA 2.5. *Let H be an eulerian graph with the maximum degree at most four and $\mathscr{Q}$ be a forbidden system of H. Suppose that $\{C', C''\}$ is a compatible cycle decomposition of $(H, \mathscr{Q})$. If C is a cycle of $SP(H, \mathscr{Q})$, then $\{C' \triangle C, C'' \triangle C\}$ is also a compatible cycle decomposition of $(H, \mathscr{Q})$. Furthermore, if $(H, \mathscr{Q})$ has some non-trivial vertex, then neither $C' \triangle C$ nor $C'' \triangle C$ is empty.*

LEMMA 2.6. *Let H be an eulerian graph with the maximum degree at most four and $\mathcal{Q}$ be a forbidden system of H. Assume that $SP(H, \mathcal{Q})$ has precisely two components R_1, R_2. Let R_i^H be the subgraph of H induced by edges of R_i $(i=1, 2)$. Then $(H, \mathcal{Q})$ is admissible if and only if $|V(R_1^H) \cap V(R_2^H)| \neq 1$.*

Lemmas 2.3, 2.5, and 2.6 follow directly from the definitions.

LEMMA 2.7. *Let G be a 4-regular graph and $\mathscr{P}$ be an admissible forbidden system of G. If each component of $SP(G, \mathscr{P})$ contains an even number of edges, then $(G, \mathscr{P})$ has a compatible circuit decomposition.*

Proof. Color an Euler tour of each component of $SP(G, \mathscr{P})$ red and blue alternatively. Then the set of all mono-colored circuits in G is a CCD of $(G, \mathscr{P})$. ▮

DEFINITION 2.8. Let P be a forbidden part of $(G, \mathscr{P})$ with $P = \{e, e'\}$. *Discharging* P is the operation on $\mathscr{P}$ of replacing P with $\{e\}, \{e'\}$ in $\mathscr{P}$, and the new system is said to be *obtained from $\mathscr{P}$ by discharging P*. For a non-trivial vertex $v \in V(G)$, *discharging at* v is the operation on $\mathscr{P}$ of discharging every forbidden part incident with v.

DEFINITION 2.9. Let $v \in V(G)$. A sequence of edge-disjoint circuits $\{C_1, ..., C_k\}$ $(k \geqslant 2)$ is a *circuit chain closed* at v if

(1) for each $i, j \in \{1, ..., k\}$ with $i \neq j$, $[V(C_i) \cap V(C_j)] \backslash \{v\} \neq \varnothing$ if and only if $j - i = \pm 1$,

(2) $v \in V(C_1) \cap V(C_k)$.

The *length* of the circuit chain $\{C_1, ..., C_k\}$ is k.

LEMMA 2.10. *Let $(G, \mathscr{P})$ be a minimal contra-pair. Assume that $(G, \mathscr{P})$ has a forbidden part P_0 with $|P_0| = 2$. Then*

(1) *the maximum degree of G is four and $|P| \leqslant 2$ for each $P \in \mathscr{P}$;*

(2) *for each forbidden part P with $|P| = 2$, and forbidden system $\mathscr{P}_P$ obtained from $\mathscr{P}$ by discharging P, every compatible circuit decomposition of $(G, \mathscr{P}_P)$ is a circuit chain closed at v where $P \in \mathscr{P}(v)$.*

Proof. By the minimality of $(G, \mathscr{P})$, G is 2-connected. Let P be a forbidden part incident with v and $|P| = 2$. Let $\mathscr{P}_P$ be the forbidden system obtained from $\mathscr{P}$ by discharging P. Clearly, $(G, \mathscr{P}_P)$ is admissible and $(G, \mathscr{P}_P) \prec (G, \mathscr{P})$. Since $(G, \mathscr{P})$ is a minimal contra-pair, it follows that $(G, \mathscr{P}_P)$ has a CCD, say $\mathscr{F}_P$. Since $(G, \mathscr{P})$ is a contra-pair, we have $|E(C) \cap P| \leqslant 1$ for every $C \in \mathscr{F}_P$ and every $P \in \mathscr{P}$, except for one $C^* \in \mathscr{F}_P$ in which $|E(C^*) \cap P| = 2$.

Construct an auxiliary graph A with the vertex set $V(A) = \mathscr{F}_P$ and two vertices of A are adjacent to each other if and only if their corresponding circuits of $\mathscr{F}_P$ have a non-empty intersection in $G\backslash\{v\}$. Since G is 2-connected, A is connected. Let $S = C_1 \cdots C_k$ be a shortest path in A joining $C^* = C_1$ and C_k where $C_k \in \mathscr{F}_P\backslash\{C_1\}$ is a circuit containing the vertex v. Obviously, $\{C_1, ..., C_k\}$ is a circuit chain of G closed at v. Let H be the subgraph of G induced by the edges of $\{C_1, ..., C_k\}$. Since the maximum degree of H is four and H is 2-connected, we see that $(H, \mathscr{P} \mid H)$ is admissible (by Lemma 2.3). If $H \neq G$, then by the minimality of $(G, \mathscr{P})$, $(H, \mathscr{P} \mid H)$ has a CCD, which together with the circuits of $\mathscr{F}\backslash\{C_1, ..., C_k\}$ forms a CCD of $(G, \mathscr{P})$. This is impossible. Therefore, $H = G$ and we have proved (1) and (2). ∎

Let $(G, \mathscr{P})$ be a minimal contra-pair containing a forbidden part P with $|P| = 2$. For each non-trivial vertex $v \in V(G)$, by Lemma 2.10, we can see that $\mathscr{P}(v)$ consists of three forbidden parts, two of them are trivial. Thus, *discharging a non-trivial forbidden part $P \in \mathscr{P}(v)$ is equivalent to discharging the non-trivial vertex v.*

LEMMA 2.11. *Let $(G, \mathscr{P})$ be a minimal contra-pair and suppose that G is 4-regular. Then*

(1) *$SP(G, \mathscr{P})$ (see Definition 2.4) has exactly two components. Furthermore,*

(2) *for each non-trivial vertex v, if x and y are the two vertices in $SP(G, \mathscr{P})$ which are split from v, then they are contained in different components of $SP(G, \mathscr{P})$.*

Proof. Let $\mathscr{F}_v$ be a CCD of $(G, \mathscr{P}_v)$ where $\mathscr{P}_v$ is obtained from $\mathscr{P}$ by discharging at a non-trivial vertex v. By Lemma 2.10, $\mathscr{F}_v$ is a circuit chain, say $\{C_1, ..., C_k\}$, closed at $v \in V(C_1) \cap V(C_k)$. Color the edges of $E(C_1) \cup E(C_3) \cup \cdots \cup E(C_{2i-1}) \cup \cdots$ *red*, and the edges of $E(C_2) \cup E(C_4) \cup \cdots \cup E(C_{2i}) \cup \cdots$ *blue*. It is easy to see that each component of $SP(G, \mathscr{P})$ containing neither x nor y has a red-blue alternatively colored Euler tour, therefore, has an even number of edges. If x and y are contained in the same component R of $SP(G, \mathscr{P})$, then R has also an even number of edges. By Lemma 2.7, $(G, \mathscr{P})$ has a CCD. This contradicts that $(G, \mathscr{P})$ is a contra-pair. Thus, *x and y are contained in different components of $SP(G, \mathscr{P})$.*

Let $R_1, ..., R_h$ be the components of $SP(G, \mathscr{P})$ where $|E(R_1)| \equiv |E(R_2)| \equiv 1 \bmod 2$ and $|E(R_i)| \equiv 0 \bmod 2$ for $i > 2$. Since the non-trivial vertex v is arbitrary chosen, with the above argument, we have already proved that *for each non-trivial vertex v of $(G, \mathscr{P})$, let x and y be the two vertices in $SP(G, \mathscr{P})$ which are split from v, each of $\{R_1, R_2\}$ must contain one of $\{x, y\}$.* So, each edge e incident with a non-trivial vertex must be contained

in either R_1 or R_2. Furthermore, no edge of R_i with $i>2$ is incident with a non-trivial vertex. By the definition of $SP(G, \mathscr{P})$, each of R_i with $i>2$ is also a component of G whose vertices are all trivial. This contradicts that G is a 2-connected (also contradicts that $(G, \mathscr{P})$ is a minimal contra-pair). Therefore, there exists no such component of even size in $SP(G, \mathscr{P})$ and this proves the lemma. ▮

LEMMA 2.12. *Let $(G, \mathscr{P})$ be a minimal contra-pair and G be 4-regular. Let $\mathscr{P}_v$ be the forbidden system obtained from $\mathscr{P}$ by discharging at some non-trivial vertex v. If $\mathscr{F}_v$ is a compatible circuit decomposition of $(G, \mathscr{P}_v)$ with $|\mathscr{F}_v|$ maximum, then $\mathscr{F}_v$ is a circuit chain of length at least three.*

Proof. The length k of $\mathscr{F}_v = \{C_1, ..., C_k\}$ is greater than one since v is of degree four and $\mathscr{F}_v$ is closed at v. Assume that $k=2$. Let R_1 and R_2 be the components of $SP(G, \mathscr{P})$. By Lemma 2.11 and Definition 2.4, without loss of generality, let $E(v) \cap E(C_1) \subseteq E(R_1)$ and let $E(v) \cap E(C_2) \subseteq E(R_2)$. Consider $\{C_1 \triangle R_1, C_2 \triangle R_1\}$. By Lemma 2.5, it is also a compatible cycle decomposition of $(G, \mathscr{P}_v)$. Note that $E(v) \subseteq E(C_2 \triangle R_1)$. The maximum degree of the cycle $C_2 \triangle R_1$ is four and hence any of its circuit decomposition consists of at least two circuits. Since $SP(G, \mathscr{P})$ has two components and $\mathscr{P}$ is admissible, by Lemma 2.6, there are at least two non-trivial vertices in $(G, \mathscr{P})$. so, by Lemma 2.5 again, $C_1 \triangle R_1 \neq \varnothing$. Thus, the union of circuit decompositions of $C_1 \triangle R_1$ and $C_2 \triangle R_1$ has at least three elements. This contradicts the maximality of $|\mathscr{F}_v|$ among all CCD's of $(G, \mathscr{P}_v)$. ▮

LEMMA 2.13. *Let $(G, \mathscr{P})$ be a minimal contra-pair and G be 4-regular. Let $\mathscr{P}_v$ be the forbidden system obtained from $\mathscr{P}$ by discharging at some non-trivial vertex v, and $\mathscr{F}_v = \{C_1, ..., C_k\}$ be a CCD (a circuit chain) of $(G, \mathscr{P}_v)$. Let H be the subgraph of G induced by $E(C_i) \cup E(C_{i+1})$ $(i=1, ..., k-1)$. If $\mathscr{F}_v = \{C_1, ..., C_k\}$ has been chosen so that $|\mathscr{F}_v| = k$ is as large as possible, then $SP(H, \mathscr{P} \mid H)$ is connected.*

Proof. Assume that $SP(H, \mathscr{P} \mid H)$ is not connected. So, $SP(H, \mathscr{P} \mid H)$ contains some non-trivial vertex. Set $V_1 = V(C_i) \cap V(C_{i-1})$ if $i \geqslant 2$ or $V_1 = \{v\}$ if $i=1$, and $V_2 = V(C_{i+1}) \cap V(C_{i+2})$ if $i+2 \leqslant k$ or $V_2 = \{v\}$ if $i+1=k$. For any $v_1 \in V_1$ and any $v_2 \in V_2$, we claim that

$$v_1, v_2 \text{ are contained in the same component of } SP(H, \mathscr{P} \mid H).$$

Assume that a component Q of $SP(H, \mathscr{P} \mid H)$ contains exactly one of them, say $v_1 \in V(Q)$ and $v_2 \notin V(Q)$, let C be a circuit containing v_1 in Q. By Lemma 2.5, $\{C_i \triangle C, C_{i+1} \triangle C\}$ is a compatible cycle decomposition of $(H, \mathscr{P} \mid H)$. Let $\mathscr{F}^*$ be the union of circuit decompositions of $C_i \triangle C$ and

$C_{i+1} \triangle C$. Since $[\mathscr{F}_v \backslash \{C_i, C_{i+1}\}] \cup \mathscr{F}^*$ is a CCD of $(G, \mathscr{P}_v)$, by the maximality of $|\mathscr{F}_v|$, we must have that $|\mathscr{F}^*| = 2$. By Lemma 2.5 again, both $C_i \triangle C$ and $C_{i+1} \triangle C$ are non-empty since $(H, \mathscr{P} \mid H)$ contains some non-trivial vertex. Thus, both $C_i \triangle C$ and $C_{i+1} \triangle C$ are circuits. Note that the circuit $C_{i+1} \triangle C$ contains both v_1, v_2. Thus, $\mathscr{F}' = [\mathscr{F}_v \backslash \{C_i, C_{i+1}\}] \cup \{C_{i+1} \triangle C\}$ is a circuit chain closed at v, but the CCD $[\mathscr{F}_v \backslash \{C_i, C_{i+1}\}] \cup \mathscr{F}^*$ is not a circuit chain. This contradicts Lemma 2.10 (2).

If $SP(H, \mathscr{P} \mid H)$ has more than one component, then there must be a component Q' such that $(V_1 \cup V_2) \cap V(Q') = \varnothing$. By the definition of V_1 and V_2, Q' is also a component of $SP(G, \mathscr{P})$ and contains neither x nor y where x and y are two vertices in $SP(G, \mathscr{P})$ split from v. This contradicts Lemma 2.11. Therefore, $SP(H, \mathscr{P} \mid H)$ is connected, as required. ∎

3. PLANAR GRAPHS

In this section, we present a pioneer result (Theorem 3.1) by Fleischner. Since this result will be used in the proof of Theorem 4.2, for completeness, we present it with an alternative proof.

THEOREM 3.1 (Fleischner [4]). *Let G be an eulerian graph and $\mathscr{P}$ be an admissible forbidden system on G. If $|P| \leqslant 2$ for each $P \in \mathscr{P}$ and G is planar, then $(G, \mathscr{P})$ has a compatible circuit decomposition.*

Proof. Suppose, to the contrary, that the theorem is false. Let $(G, \mathscr{P})$ be a counterexample with $|E(G)|$ as small as possible among all the minimal contra-pairs. By Lemma 2.10, $d(v) \leqslant 4$ for all $v \in V(G)$. It follows from the minimality of $|E(G)|$ that G is 4-regular. By Lemma 2.11, let R_1, R_2 be the two components of $SP(G, \mathscr{P})$ and let R_i^G be the subgraph of G induced by the edges of R_i $(i = 1, 2)$.

(I) The theorem needs no proof if a graph has no non-trivial vertex since any circuit decomposition of G is a CCD of $(G, \mathscr{P})$, and by Lemma 2.6, $(G, \mathscr{P})$ *has at least two non-trivial vertices.*

(II) Let G be embedded in a plane. A non-trivial vertex v of $(G, \mathscr{P})$ is called a *$\mathscr{P}$-crossing vertex* if there is a $P_1 = \{e', e''\} \in \mathscr{P}(v)$ such that e' and e'' are not consecutive on the boundary of any face.

We claim that $(G, \mathscr{P})$ *has no $\mathscr{P}$-crossing vertex*. Assume that v is a $\mathscr{P}$-crossing vertex of $(G, \mathscr{P})$. Let $E(v) = \{e_1, e_2, e_3, e_4\}$ be arranged on the plane in the cyclic order as e_1, e_2, e_3, e_4, e_1. Without loss of generality, let $\mathscr{P}(v) = \{\{e_1, e_3\}, \{e_2\}, \{e_4\}\}$. Let $\mathscr{F}_v$ be a CCD-of $(G, \mathscr{P}_v)$ where $\mathscr{P}_v$ is obtained from $\mathscr{P}$ by discharging at v and $\mathscr{F}_v$ is chosen so that $|\mathscr{F}_v|$ is as larger as possible. By Lemma 2.10, $\mathscr{F}_v = \{C_1, ..., C_k\}$ is a circuit chain

closed at v. Without loss of generality, let $e_1, e_3 \in E(C_1)$ and $e_2, e_4 \in E(C_k)$. Thus, C_1 and C_k "cross" each other on the plane at the vertex v. Since both C_1 and C_k are circuits, they must "cross" each other again on the plane at another vertex. Thus, by the definition of circuit chain, $k=2$ since $|V(C_1) \cap V(C_k)| \geqslant 2$. This contradicts Lemma 2.12 and proves our claim.

(III) We claim that $(G, \mathscr{P})$ *has no trivial vertex*. Assume that v is a trivial vertex of $(G, \mathscr{P})$. Let $E(v) = \{e_1, ..., e_4\}$ and the edges of $E(v)$ are embedded on the plane in the cyclic order as e_1, e_2, e_3, e_4, e_1. Since v is trivial, without loss of generality, let $E(v) \subseteq E(R_1^G)$. Since R_1^G is a cycle of G, we can split a pair of edges e_i, e_{i+1} $(i \in \{1, 2\})$ away from v by preserving R_1^G as a connected cycle, and replacing the edges e_i, e_{i+1} with a single edge e'. Let G' be the resulting graph and consider $\mathscr{P}$ as a forbidden system of G'. By Lemma 2.6, $(G', \mathscr{P})$ is admissible. Let $\mathscr{F}$ be CCD of $(G', \mathscr{P})$ since $|E(G')| < |E(G)|$. It is obvious that $\mathscr{F}$ is also at compatible cycle decomposition of $(G, \mathscr{P})$ (by replacing e' with the original edges e_i, e_{i+1} and identify the split vertices to the single vertex v). This is a contradiction.

(IV) Since $(G, \mathscr{P})$ has neither trivial vertex and nor $\mathscr{P}$-crossing vertex, the components R_1, R_2 of the split $SP(G, \mathscr{P})$ are two disjoint circuits on the plane. We let $R_1 = x_1 \cdots x_n x_1$ and $R_2 = y_1 \cdots y_n y_1$ where x_i and y_i are split from $v_i \in V(G) = \{v_1, ..., v_n\}$. By (I), $n \geqslant 2$. Thus, the collection of 2-circuits $v_i v_{i+1} v_i$, for all $i = 1, ..., n, \bmod n$, is a CCD of $(G, \mathscr{P})$. This contradicts the assumption that $(G, \mathscr{P})$ is a counterexample and completes the proof of the theorem. ▌

4. K_5-FREE GRAPHS

DEFINITION 4.1. Let T be a vertex-cut of a graph G separating G into two parts G_1 and G_2 that $G_1 \cap G_2 = T$ and $G_1 \cup G_2 = G$. For a cycle C of G, we say that C *crosses* $x \in T$ if $E(C) \cap E_{G_i}(x) \neq \varnothing$ for both $i = 1, 2$.

Let T be a vertex cut of an eulerian graph G. If a cycle C crosses a non-trivial vertex $x \in T$ with $d(x) = 4$, then it is obvious that $|T \cap V(C)| \geqslant 2$.

THEOREM 4.2. *Suppose that G is an eulerian graph with an admissible forbidden system $\mathscr{P}$ in which each forbidden part has cardinality at most* 2. *If G does not contain K_5 as a minor, then $(G, \mathscr{P})$ has a compatible circuit decomposition.*

Proof. Suppose, to the contrary, that the theorem is false. Let $(G, \mathscr{P})$ be a counterexample with $|E(G)|$ as small as possible among all the minimal contra-pairs. By Lemma 2.10, $d(v) \leqslant 4$ for all $v \in V(G)$. It follows from the

minimality of $|E(G)|$ that G is 4-regular. For each non-trivial vertex v, let $\mathscr{P}(v)=\{P_1, P_2, P_3\}$ with $|P_1|=2$, without causing any confusion and for the sake of convenience, we replace $\mathscr{P}(v)$ with $\{P_1, P_2 \cup P_3\}$.

(I) By Theorem 3.1, G is non-planar. A result of Halin (see Lemma 3.10 of [3, pp. 252–253]) states that every 4-connected non-planar graph contains a K_5-minor. Thus, G has a vertex cut of order at most three. Let $T=\{x_1, ..., x_t\}$ be a smallest vertex cut of G separating G into two parts G_1 and G_2 with $t=|T|\leqslant 3$.

(II) We claim that T *must have a balanced separator* (see Definition 2.2). Note that since G is eulerian and $|T|\leqslant 3$, T has either no or two odd separators. Assume that no vertex of T is balanced. Let G_T be the graph with the vertex set $V(G_T)=T$ and $\mathscr{P}_T$ be a forbidden system of G_T constructed as follows. (1) If T has two odd separators, say x_1 and x_2, then G_T is a path $e_1 \cdots e_{t-1}$ joining x_1 and x_2 and passing through all vertices of T, and $\mathscr{P}_T=\{\{e_1\}, \{e_1\}\}$ if $t=2$ and $\mathscr{P}_T=\{\{e_1\}, \{e_1, e_2\}, \{e_2\}\}$ if $t=3$; (2) If T has no odd separator, then G_T is a circuit $e_1 \cdots e_t$ containing all vertices of G_T and $\mathscr{P}_T=\{\{e_i, e_{i+1}\}: i=1, ..., t, \text{mod } t\}$.

Let $H_i=G_i \cup G_T$ and $\mathscr{P}_i=[\mathscr{P} \mid G_i] \cup \mathscr{P}_T$ for each $i=1, 2$. It is easy to see that H_i has no K_5-minor and $\mathscr{P}_i$ is admissible since H_i is 2-connected (by Lemma 2.3). Thus, $(H_i, \mathscr{P}_i)$ has a CCD $\mathscr{F}_{H_i}$. Appropriate combination of elements of $\mathscr{F}_{H_1}$ and $\mathscr{F}_{H_2}$ containing edges of G_T yields a CCD of $(G, \mathscr{P})$. This contradicts that $(G, \mathscr{P})$ is a contra-pair.

(III) *Let $x_1 \in T$ be a balanced separator*. Let $\mathscr{F}_{x_1}$ be a CCD of $(G, \mathscr{P}_{x_1})$ where $\mathscr{P}_{x_1}$ is obtained from $\mathscr{P}$ by discharging at x_1 with $|\mathscr{F}_{x_1}|$ as large as possible. By Lemma 2.10, $\mathscr{F}_{x_1}=\{C_1, ..., C_k\}$ is a circuit chain closed at x_1. By Lemma 2.12, $k\geqslant 3$ and therefore $V(C_1)\cap V(C_k)=\{x_1\}$. Since both C_1 and C_k cross $x_1 \in T$ and $t\leqslant 3$, $|V(C_j)\cap T|=2$ for both $j\in\{1, k\}$. Note that $V(C_1)\cap V(C_k)=\{x_1\}$. Without loss of generality, let $x_2 \in [V(C_1)\cap T]\backslash\{x_1\}$ and $x_3 \in [V(C_k)\cap T]\backslash\{x_1\}$. Here, we also proved that $|T|=3$ and hence, G *is* 3*-connected.*

(IV) We claim that *both x_2 and x_3 are even separators of G* and $k=3$. Let $G^*=G\backslash[\{x_1\} \cup E(C_1) \cup E(C_k)]$ which is the connected subgraph of G induced by edges contained in $\bigcup_{i=2}^{k-1} C_i$. The degree two vertices x_2 and x_3 of G^* become a 2-vertex cut of the graph G^* separating $G_1^*=G_1\backslash[\{x_1\} \cup E(C_1) \cup E(C_k)]$ and $G_2^*=G_2\backslash[\{x_1\} \cup E(C_1) \cup E(C_k)]$. Thus, x_2 and x_3 cannot be both odd separators of G for otherwise, either G^* is disconnected (when $d_{G_i}(x_2)\neq d_{G_i}(x_3)$ for both $i=1, 2$), or one of $\{V(G_1)\backslash T, V(G_2)\backslash T\}$ is empty (when $d_{G_i}(x_2)=d_{G_i}(x_3)$ for both $i=1, 2$) since $x_2 \in V(C_2)$ and $x_3 \in V(C_{k-1})$. So, each $x_i \in T$ must be an even separator.

Since C_2 crosses $x_2 \in T$, $|V(C_2) \cap T| = 2$. Note that $x_1 \in V(C_1) \cap V(C_k)$ and $k \geqslant 3$. C_2 must cross both x_2 and x_3. Therefore, $C_{k-1} = C_2$. That is, $k = 3$.

(V) Now we claim that *T has precisely two balanced separators.* Recall Lemma 2.11, let R_1 and R_2 be the components of $SP(G, \mathscr{P})$. Note that R_1 and R_2 are cycles in G. If every vertex of T is balanced, then each cycle R_1, R_2 of G must cross every vertex of T. Note that $|T| = 3$. This contradicts that R_1 and R_2 are cycles of G. So, we assume that *x_1 and x_3 are balanced and x_2 is even but not balanced.*

(VI) Now, let us recall all that we have (Fig. 1). *G is 3-connected* (by (III)), *$T = \{x_1, x_2, x_3\}$ is a vertex cut of G separating G into two parts G_1 and G_2 where x_1 and x_3 are balanced, x_2 is even and unbalanced* (by (IV) and (V)), *$\mathscr{F}_{x_1} = \{C_1, C_2, C_3\}$ is a CCD (a circuit chain) of $(G, \mathscr{P}_{x_1})$ where $x_2 \in C_1 \cap C_2$, $x_3 \in C_2 \cap C_3$, and $\{x_1\} = C_1 \cap C_3$* (by (V)). In the final step of the proof, let H be the subgraph induced by $E(C_2) \cup E(C_3)$, we will show that *the split $SP(H, \mathscr{P} \mid H)$ is not connected* which leads a contradiction to Lemma 2.13 and completes the proof of the theorem.

Let $L_{12} = C_1 \cap G_2$ which is a path joining x_1 and x_2, $L_{23} = C_2 \cap G_2$ which is a path joining x_2 and x_3, and $L_{13} = C_3 \cap G_2$ which is a path joining x_1 and x_3. For each $h \in \{1, 2, 3\}$ and $i = h, h-1 \pmod{(3)}$, let e_{hi} be the edge of C_h incident with x_i and contained in G_1. Let J_1 be the graph

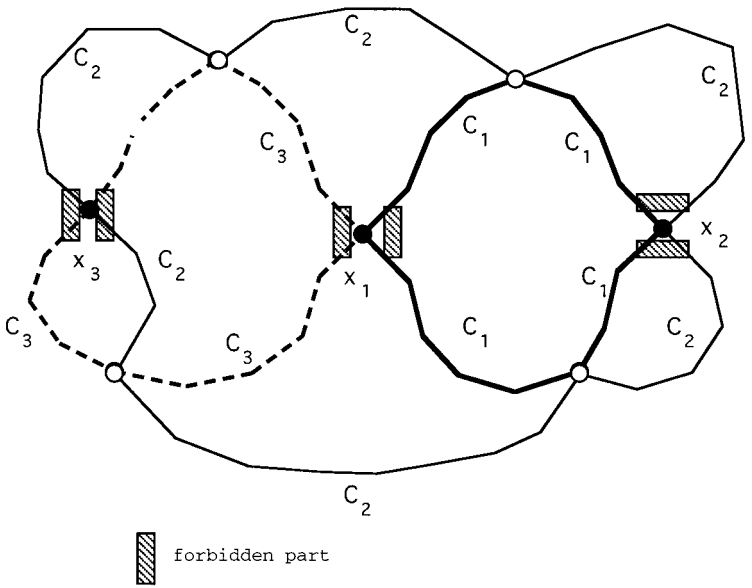

FIG. 1. The 3-cut $\{x_1, x_2, x_3\}$ and the *CCD* $\{C_1, C_2, C_3\}$ of $(G, \mathscr{P}_{x_1})$.

obtained from G_1 by adding three new edges $\{f_{ij} = x_i x_j : 1 \leqslant i < j \leqslant 3\}$ and let

$$\mathscr{Q}_1 = \left[\bigcup_{v \in V(G_1) \setminus T} \mathscr{P}(v) \right] \cup \mathscr{Q}_1(x_1) \cup \mathscr{Q}_1(x_2) \cup \mathscr{Q}_1(x_3),$$

where

$$\mathscr{Q}_1(x_1) = \{\{f_{12}, e_{11}\}, \{f_{13}, e_{31}\}\},$$
$$\mathscr{Q}_1(x_3) = \{\{f_{23}, e_{33}\}, \{f_{13}, e_{23}\}\},$$

and

$$\mathscr{Q}_1(x_2) = \{\{f_{12}, f_{23}\}, \{e_{12}, e_{22}\}\}.$$

Since $(J_1, \mathscr{Q}_1)$ is smaller than the smallest counterexample $(G, \mathscr{P})$ and contains no K_5-minor, let $\mathscr{F}_{J_1}$ be a CCD of $(J_1, \mathscr{Q}_1)$. Since $\{f_{12}, f_{23}\} \in \mathscr{Q}_1$, f_{12}, f_{23} are not contained in the same circuit of $\mathscr{F}_{J_1}$. Thus, we have the following cases.

(1) *no pair of* $\{f_{ij} : 1 \leqslant i < j \leqslant 3\}$ *is contained in the same circuit of* $\mathscr{F}_{J_1}$;

(2) f_{12}, f_{13} *are contained in the same circuit of* $\mathscr{F}_{J_1}$; and

(3) f_{13}, f_{23} *are contained in the same circuit of* $\mathscr{F}_{J_1}$.

Replacing each f_{ij} with L_{ij}, for each $1 \leqslant i < j \leqslant 3$, in each circuit of $\mathscr{F}_{J_1}$ yields a cycle decomposition $\mathscr{F}$ of $(G, \mathscr{P})$. In the first two cases, this decomposition is compatible since $L_{12} \cap L_{13} = C_1 \cap C_3 = \{x_1\}$. In the third case, let C be the circuit of $\mathscr{F}_{J_1}$ containing both f_{13} and f_{23}.

Note that $D = (C \setminus \{f_{23}, f_{13}\}) \cup (L_{23} \cup L_{13})$ is a cycle in $\mathscr{F}$. If $(D, \mathscr{P} \mid D)$ is admissible, then it has a CCD that together with $\mathscr{F} \setminus \{D\}$ is a CCD of $(G, \mathscr{P})$, a contradiction. Thus, $(D, \mathscr{P} \mid D)$ is not admissible. By Lemma 2.3, the cycle $D = (C \setminus \{f_{23}, f_{13}\}) \cup (L_{23} \cup L_{13})$ has an unbalanced, nontrivial cut-vertex y. Since C is a circuit, the unbalanced, non-trivial vertex y in D is contained $V(L_{23}) \cap V(L_{13})$ which separates x_3 from $\{x_1, x_2\}$ in $G_2 \setminus E(C_1)$.

By a symmetric argument (with G_1 and G_2 exchanging the roles), there is a non-trivial vertex $z \in V(C_3 \cap G_1) \cap V(C_2 \cap G_1)$ such that z is a cut-vertex of $G_1 \setminus E(C_1)$ which separates x_3 from $\{x_1, x_2\}$ and is unbalanced. It follows that $\{y, z\}$ is a vertex cut of $G \setminus E(C_1)$, which is induced by $E(C_2) \cup E(C_3)$. But, $SP(G \setminus E(C_1), \mathscr{P} | (G \setminus E(C_1)))$ is disconnected since both y, z are non-trivial and unbalanced. This contradicts Lemma 2.13, and completes the proof of the theorem. ∎

5. ANTI-CHAIN AND ADMISSIBILITY

Let G be an eulerian graph and $\mathscr{P}$ be a forbidden system of G. Let $v^* \in V(G)$ and $P^* \in \mathscr{P}(v^*)$ with $|P^*| \geqslant 2$ and $e^* \in P^*$. Let

$$\mathscr{P}' = [\mathscr{P} \backslash \{P^*\}] \cup \{P^* \backslash \{e^*\}, \{e^*\}\}.$$

Assume that $(G, \mathscr{P}')$ has a compatible cycle decomposition $\mathscr{F}$ and one circuit C^* of $\mathscr{F}$ contains two edges of P^*, one of which is e^*. A cycle $C \in \mathscr{F}$ is *bad* if $|E(C) \cap P^*| = 1$, and is *good* otherwise. A compatible cycle decomposition $\mathscr{F}$ of $(G, \mathscr{P}')$ is *special* if each bad cycle of $\mathscr{F}$ is a circuit, and each good cycle is connected. The cycle of $\mathscr{F}$ containing the edge e^* is denoted by C^*.

Following the argument used by Seymour [8], we are to study the relation between the admissibility of $(G, \mathscr{P})$ and a special compatible cycle decomposition $\mathscr{F}$ of $(G, \mathscr{P}')$. Construct an auxiliary digraph $G^d_{\mathscr{F}} = (V, A)$ as

$$V(G^d_{\mathscr{F}}) = V(G), \qquad A(G^d_{\mathscr{F}}) = \bigcup_{C \in \mathscr{F}} A(T_C),$$

where, for each bad circuit $C \in \mathscr{F}$, T_C is a transitive tournament with the vertex set $V(C) \backslash \{v^*\}$ and a Hamilton dipath $C \backslash \{v^*\}$ starting at w (where $\{v^* w\} = P^* \cap E(C)$), and for each good (connected) cycle $C \in \mathscr{F}$, T_C is a complete digraph on $V(C)$. An arc a of $G^d_{\mathscr{F}}$ is said to be *induced by a cycle* C if $a \in A(T_C)$. An *admissible dipath closed at* v^* in $G^d_{\mathscr{F}}$ is a directed path $Q = x_0 \cdots x_k$ such that $x_0 = x_k = v^*$ and the arc $x_{k-1} x_k$ is induced by C^* and $x_0 x_1$ is induced by a good cycle of $\mathscr{F}$ other than C^*. The *length* of an admissible dipath Q is the number of arcs contained in Q.

The following lemma is adapted from [8] which was originally for faithful cycle cover problem.

LEMMA 5.1. *Let G, $\mathscr{P}$ and $\mathscr{F}$, etc. be defined as above. Then $(G, \mathscr{P})$ is admissible if and only if $G^d_{\mathscr{F}}$ has an admissible dipath closed at v^*.*

Proof. ($\Leftarrow$) In order to prove that $(G, \mathscr{P})$ is admissible, we only need to check those edge-cuts T that intersect with the forbidden part P^* since $(G, \mathscr{P}')$ has a compatible cycle decomposition $\mathscr{F}$. Assume that $(G, \mathscr{P})$ is not admissible. That is, the graph G has an edge-cut T' that

$$|P^* \cap T'| > |T' \backslash P^*|.$$

Let $\mathscr{F}'$ be the subset of $\mathscr{F}$ such that each $C \in \mathscr{F}'$ contains some edges of T'. Note that for each $C \in \mathscr{F}' \setminus \{C^*\}$,

$$|C \cap (P^* \cap T')| \leqslant |C \cap (T' \setminus P^*)|$$

since $\mathscr{F}$ is a compatible cycle decomposition of $(G, \mathscr{P}')$. Because of $|P^* \cap T'| > |T' \setminus P^*|$, it is obvious that $C^* \in \mathscr{F}'$ and every $C \in \mathscr{F}' \setminus \{C^*\}$ is a bad circuit with

$$|C \cap (P^* \cap T')| = |C \cap (T' \setminus P^*)| = 1.$$

Let $\{X', Y'\}$ be the partition of $V(G)$ such that T' consists of all edges joining X' and Y' with $v^* \in X'$ and $w \in Y'$ for each $v^*w \in P^* \cap T'$. Thus, in of the auxiliary digraph $G^d_{\mathscr{F}}$, there are precisely two arcs oriented from X' to Y' (each of which is induced by C^*) and all other arcs joining X' and Y' are oriented from Y' to X'. Since the admissible dipath $Q = x_0 \cdots x_k$ contains the arc $x_{k-1}x_k = x_{k-1}v^*$ which is induced by C^* and is oriented from Y' to X', $Q \cap T'$ must contain another arc oriented from X' to Y'. But the only two arcs oriented from X' to Y' are induced by C^* and incident with v^*. This contradicts the definition of the admissible dipath Q.

($\Rightarrow$) Let

$$X''_o = \{x : v^*x \in E(v^*) \setminus P^* \text{ and is not contained in any bad circuit of } \mathscr{F}\}.$$

Since $(G, \mathscr{P})$ is admissible, we have that

$$|P^*| \leqslant \frac{d(v^*)}{2}.$$

Therefore, there is a good cycle of $\mathscr{F}$ that contains at least two edges of $E(v^*) \setminus P^*$ because $|C^* \cap P^*| = 2$ and $|C \cap P^*| = 1$ for every bad circuit $C \in \mathscr{F}$. That is, $|X''_o| \geqslant 2$.

Let $\{v^*w_1, v^*w_2\} = C^* \cap P^*$. Let Y'' be the set consisting of all vertices $y \in V(G^d_{\mathscr{F}}) = V(G)$ that there is a dipath in $G^d_{\mathscr{F}}$ from y to $\{w_1, w_2\}$. If $X''_o \cap Y'' \neq \varnothing$, then $G^d_{\mathscr{F}}$ has an admissible dipath closed at v^*. So, we assume that $X''_o \cap Y'' = \varnothing$. Let $X'' = V(G) \setminus Y''$.

Let $\mathscr{F}''$ be the subset of $\mathscr{F}$ such that each $C \in \mathscr{F}''$ induces some arc of $G^d_{\mathscr{F}}$ joining X'' and Y''. By the choice of Y'', all arcs joining X'' and Y'' in $G^d_{\mathscr{F}}$, except for v^*w_1 and v^*w_2, are oriented from Y'' to X''. Thus, for every good cycle $C \in \mathscr{F} \setminus \{C^*\}$, either $V(C) \subseteq X''$ or $V(C) \subseteq Y''$, and $V(C^*) \setminus \{v^*\} \subseteq Y''$. Furthermore, every cycle of $\mathscr{F}'' \setminus \{C^*\}$ is a bad circuit and passes thorough the edge cut $T'' = [X'', Y'']$ of G precisely twice: once in P^* and once in $T'' \setminus P^*$. Hence

$$|P^* \cap T''| = |\mathscr{F}'' \setminus \{C^*\}| + 2$$

and

$$|T''\backslash P^*| = |\mathscr{F}''\backslash\{C^*\}|.$$

This contradicts that $(G, \mathscr{P})$ is admissible since $|P^* \cap T''| \geqslant |T''\backslash P^*|$. ∎

Let $Q = x_0 \cdots x_k$ be an admissible dipath of $G^d_{\mathscr{F}}$ and let $S_Q = C_1 \cdots C_k$ be a sequence of cycles that $C_i \in \mathscr{F}$ is the cycle that induces the arc $x_{i-1}x_i$ (for $i = 1, ..., k$). The sequence S_Q is called an *anti-chain of* $(G, \mathscr{P}')$ *closed at* v^* *and induced by* Q.

6. FORBIDDEN SYSTEM REDUCTION

Let $(G, \mathscr{P})$ be a minimal contra-pair. By the minimality of $(G, \mathscr{P})$, G is 2-connected. Since $(G, \mathscr{P})$ is a contra-pair, it contains non-trivial forbidden parts. Let

$$r = \min\{|P|: P \in \mathscr{P} \text{ and } |P| \geqslant 2\}$$

and let P^* be a forbidden part incident with a vertex v^* such that $|P^*| = r$. Let $e \in P^*$. Set $P' = \{e^*\}$ and $P'' = P^*\backslash\{e^*\}$. Define $\mathscr{P}' = (\mathscr{P}\backslash\{P^*\}) \cup \{P', P''\}$. Clearly, $(G, \mathscr{P}')$ is admissible and $(G, \mathscr{P}') \prec (G, \mathscr{P})$. Since $(G, \mathscr{P})$ is minimal, it follows that $(G, \mathscr{P}')$ has a CCD. It is obvious that each special compatible cycle decomposition of $(G, \mathscr{P}')$ has $r-2$ bad circuits.

By Lemma 5.1, for each special compatible cycle decomposition $\mathscr{F}$ of $(G, \mathscr{P}')$, there is an admissible dipath $Q = x_0 \cdots x_k$ closed at v^* in $G^d_{\mathscr{F}}$ and an anti-chain $S_Q = C_1 \cdots C_k$ induced by Q (where the auxiliary graph $G^d_{\mathscr{F}}$, the admissible dipath Q and the anti-chain S_Q are as defined in Section 5).

We present a few lemmas to describe the structure of the minimal contra-pair $(G, \mathscr{P})$ before the final proof of Theorem 6.5. In the following Lemmas 6.1, 6.2, 6.3, and 6.4, the ordered pairs $(G, \mathscr{P})$ and $(G, \mathscr{P}')$ are those defined above.

LEMMA 6.1. *For each special compatible cycle decomposition* $\mathscr{F}$ *of* $(G, \mathscr{P}')$ *and each admissible dipath* Q *of* $G^d_{\mathscr{F}}$ *closed at* v, *every element of* $\mathscr{F}$ *must appear at least once in the anti-chain* S_Q *which is induced by* Q.

Proof. Assume that an element $C \in \mathscr{F}$ does not appear in S_Q. Let $H = G\backslash E(C)$. Since Q remains as an admissible dipath in $H^d_{\mathscr{F}\backslash\{C\}}$, by Lemma 5.1, $(H, \mathscr{P} \mid H)$ is admissible. Note that $(H, \mathscr{P} \mid H) \prec (G, \mathscr{P})$. Let $\mathscr{F}'$ be a CCD of $(H, \mathscr{P} \mid H)$. Then $\mathscr{F}' \cup \{C\}$ is a compatible cycle decomposition of $(G, \mathscr{P})$. This contradicts that $(G, \mathscr{P})$ is a contra-pair and proves the lemma. ∎

LEMMA 6.2. *Let $\mathscr{F}$ be a special compatible cycle decomposition of $(G, \mathscr{P}')$. Let $Q = x_0 \cdots x_k$ be a* shortest *admissible dipath of $G^d_{\mathscr{F}}$ closed at v^*, and let $S_Q = C_1 \cdots C_k$ be the anti-chain induced by Q. Then,*

(1) *each vertex is contained in at most two good cycles of $\mathscr{F}$;*

(2) *for each pair of good cycles C_i and C_j,*

$$C_i \cap C_j \neq \varnothing$$

if and only if $i = j \pm 1$, except that $V(C_1) \cap V(C_k) = \{v^*\}$;

(3) *for each good cycle C_μ of $\mathscr{F}$, $V(C_\mu) \cap \{x_0, ..., x_k\} = \{x_{\mu-1}, x_\mu\}$ and hence C_μ appears precisely once in the anti-chain S_Q.*

Proof. Assume that C_i and C_j are two good cycles with $j > i+1$ and $V(C_i) \cap V(C_j) \neq \varnothing$. Let $x^* \in V(C_i) \cap V(C_j)$. Then $Q^* = x_0 \cdots x_{i-1} x^* x_j \cdots x_k$ is an admissible dipath of $G^d_{\mathscr{F}}$ shorter than Q. This contradicts our choice of Q and proves (1) and (2).

Assume that $x_\alpha \in V(C_\mu) \cap \{x_0, ..., x_k\}$ and $x_\alpha \notin \{x_{\mu-1}, x_\mu\}$. Without loss of generality, let $\alpha > \mu$. Then $Q^{**} = x_0 \cdots x_{\mu-1} x_\alpha \cdots x_k$ is an admissible dipath of $G^d_{\mathscr{F}}$ shorter than Q. This contradicts our choice of Q and proves the lemma. ∎

LEMMA 6.3. (1) *$d(v) \leqslant 2r$, for each vertex v of G and*

(2) *$|P| = r$, for each non-trivial forbidden part $P \in \mathscr{P}$.*

Proof. Let $\mathscr{F}$ be a CCD of $(G, \mathscr{P}')$ (note that each element of $\mathscr{F}$ is a circuit in this proof). By Lemma 6.2 (1), each vertex of G is contained in at most two good circuits. Since $\mathscr{F}$ has precisely $r-2$ bad circuits, each vertex is contained in at most r circuits. Therefore, $d(v) \leqslant 2r$.

Since $d(v) \leqslant 2r$ and $(G, \mathscr{P})$ is admissible, $|P| \leqslant r$ for each $P \in \mathscr{P}$. By the choice of P^*, we have that $|P| = r$ for each non-trivial forbidden part $P \in \mathscr{P}$. ∎

As an immediate corollary of Lemma 6.3 and Lemma 6.2 (1), we have the following lemma.

LEMMA 6.4. *For each special compatible cycle decomposition $\mathscr{F}$ of $(G, \mathscr{P}')$,*

(1) *each non-trivial forbidden part P intersects all $(r-2)$ bad circuits and precisely two good cycles of $\mathscr{F}$,*

(2) *and $d_C(v) = 2$ for every non-trivial vertex v and every element C of $\mathscr{F}$ containing v.*

In the proof of Theorem 6.5, we need one more lemma (Lemma 6.6) which is very technical and deals with the local structure of a minimal contra-pair. Due to its complicated description, we suggest that readers read the lemma when it is needed in the proof of Theorem 6.5 so that they may have a clear view and a better understanding of the lemma.

THEOREM 6.5. *If* $(G, \mathscr{P})$ *is a minimal contra-pair, then every forbidden part has cardinality at most* 2 *and every vertex has degree at most* 4.

Proof. We continue the discussion at the beginning of this section. Among all special compatible cycle decompositions $\mathscr{F}$ of $(G, \mathscr{P}')$ and among all admissible dipaths Q of $G^d_{\mathscr{F}}$, we choose a special compatible cycle decomposition $\mathscr{F}_0$ of $(G, \mathscr{P}')$ and an admissible dipath $Q_0 = x_0 \cdots x_k$ of $G^d_{\mathscr{F}_0}$ such that Q_0 is *shortest*.

If $r = 2$, the theorem follows from Lemma 2.10 (1). We assume that $r \geqslant 3$. Thus, $\mathscr{F}_0$ has some bad circuit.

Let $C_a = v_0 \cdots v_s$ be the bad circuit of $\mathscr{F}_0$ with the subscript a as small as possible where $v_0 = v_s = v^*$ and $\{v_0 v_1\} = E(C_a) \cap P^*$. Since C_1 is a good cycle, $a \geqslant 2$. Note that the arc $x_{a-1}x_a$ of Q_0 is induced by the bad circuit C_a. Let

$$v_m = x_{a-1} \qquad \text{and} \qquad v_n = x_a,$$

where $0 < m < n < s$. For the sake of convenience, we choose $m = \min\{i : v_i \in V(C_a) \cap V(C_{a-1})\}$. Let G_a be the subgraph of G induced by $E(C_a) \cup E(C_{a-1})$. And denote the restriction of $\mathscr{P}$ on G_a by $\mathscr{P}_a$. In the proof, we are to study the structure of $(G_a, \mathscr{P}_a)$ and then we will find another compatible cycle decomposition $\mathscr{F}_a$ of $(G_a, \mathscr{P}_a)$ such that an admissible dipath in $G^d_{\mathscr{F}'}$ closed at v^* is shorter than Q_0 where $\mathscr{F}' = [\mathscr{F}_0 \setminus \{C_{a-1}, C_a\}] \cup \mathscr{F}_a$. This contradicts the choice of Q_0 and finally proves the theorem.

(I) By the choice of $x_{a-1} = v_m$, we have that $d_{G_a}(v) = 2$ *for each internal vertex* v *of the segment* $v_0 \cdots v_m$ *of* C_a.

Since $v_n = x_a \in V(Q_0)$, by Lemma 6.2 (3), $v_n \notin V(C_{a-1})$. Thus $d_{G_a}(v_n) = 2$ since C_a is a circuit.

(II) Note that a bad circuit may appear in the anti-chain S_{Q_0} more than once. We claim that *for each arc* $x_{b-1}x_b$ *of* Q_0 *induced by the bad circuit* $C_a = C_b$ *with* $b > a$, x_{b-1} *and* x_b *are contained in the segment* $v_1 \cdots v_{m-1}$ *of* C_a.

Since $x_{b-1}x_b$ is an arc in the transitive tournament T_{C_a}, let $x_{b-1} = v_p$ and $x_b = v_q$ with $p < q$. Assume that $v_q = x_b$ is contained in the segment $v_m \cdots v_{s-1}$ of C_a. If $q > m$, there is an arc $v_m v_q = x_{a-1}x_b$ in the transitive tournament T_{C_a}. Thus, either $x_0 \cdots x_{a-1}x_b \cdots x_k$ (if $q > m$) or

$x_0 \cdots x_{a-1} x_{b+1} \cdots x_k$ (if $q = m$) is an admissible dipath in $G^d_{\mathscr{F}_0}$ shorter than Q_0. This contradicts the choice of Q_0 and proves our claim. For any compatible circuit decomposition $\mathscr{F}_a$ of $(G_a, \mathscr{P}_a)$, let $D_1 \in \mathscr{F}_a$ be the circuit containing the edge $v_0 v_1$ ($\in P^* \cap E(G_a)$). By I., the segment $v_0 \cdots v_m$ of C_a remains as a segment in D_1. Thus,

($\bigstar$) *for any special cycle decomposition* $\mathscr{F}_a$ *of* $(G_a, \mathscr{P}_a)$, *the segments* $x_0 \cdots x_{a-2}$ *and* $x_a \cdots x_k$ *of* Q_0 *remain as dipaths in* $G^d_{\mathscr{F}'}$, *where* $\mathscr{F}' = [\mathscr{F}_0 \backslash \{C_a, C_{a-1}\}] \cup \mathscr{F}_a$.

(III) We claim that $(G_a, \mathscr{P}_a)$ *must contain some non-trivial vertex.*

If $a \geqslant 3$, we first show that *there must be some non-trivial vertex of* $(G, \mathscr{P})$ *contained in* $V(C_{a-1}) \cap V(C_{a-2})$. Suppose not, then $C_{a-1} \cup C_{a-2}$ is a connected good cycle and we can replace C_{a-1}, C_{a-2} in $\mathscr{F}_0$ with $C_{a-1} \cup C_a$. Thus, in the resulting digraph $G^d_{\mathscr{F}_0}$, we have a shorter admissible dipath $x_0 \cdots x_{a-3} x_{a-1} \cdots x_k$. This contradicts the choice of $\mathscr{F}_0$ and Q_0. Since every non-trivial forbidden part of $(G, \mathscr{P})$ must intersect with every bad circuit of $\mathscr{F}_0$ (by Lemma 6.4 (1)), a non-trivial vertex of $(G, \mathscr{P})$ contained in $V(C_{a-2}) \cap V(C_{a-1})$ is also contained in $V(C_a)$ and is therefore a non-trivial vertex of $(G_a, \mathscr{P}_a)$.

Assume that $a = 2$ and all vertices of G_a are trivial with respect to $\mathscr{P}_a$. Let P_1 be a path contained in the connected cycle C_1 ($= C_{a-1}$) joining $v^* = v_0$ and v_m, and P_2 be the segment $v_m \cdots v_s$ of C_2 ($= C_a$) passing through $v_n = x_a$ ($= x_2$). Let $D_1 = P_1 \cup P_2$, and $\{D_2, ...\}$ be a circuit decomposition of $G_a \backslash E(D_1)$. Then $\mathscr{F}_1 = [\mathscr{F}_0 \backslash \{C_1, C_2\}] \cup \{D_1, D_2, ...\}$ is a special compatible cycle decomposition of $(G, \mathscr{P}')$. Note that, by ($\bigstar$), $x_2 \cdots x_k$ remains as a dipath in $G^d_{\mathscr{F}_1}$. Since $v^* v_n = x_0 x_2$ is an arc in the complete digraph T_{D_1}, we obtain an admissible dipath $x_0 x_2 \cdots x_k$ in $G^d_{\mathscr{F}_1}$, which is shorter than Q_0. This is a contradiction.

(IV) We claim that *for each non-trivial vertex* u *of* $(G_a, \mathscr{P}_a)$,

(i) $d_{C_a}(u) = 2$, $d_{C_{a-1}}(u) = 2$ *and* $d_{G_a}(u) = 4$;

(ii) $u \in V(C_{a-2})$ *and* $a \geqslant 3$;

(iii) $u \in \{v_{n+1}, ..., v_{s-1}\}$.

Part (i) follows from Lemma 6.4 (2). Part (ii) follows from Lemma 6.4 (1) and Lemma 6.2 (2). For the proof of (iii), since $d_{G_a}(v_n) = 2$, $u \neq v_n = x_a$. Note that $v_0 = v_s = v^*$ is trivial in $(G_a, \mathscr{P}_a)$ since the only non-trivial forbidden part P^* incident with $v_0 = v_s = v^*$ contains only one edge $v_0 v_1$ of G_a. Thus, $u \neq v_0 = v_s$. Assume that $u \in \{v_1, ..., v_{n-1}\}$. By (ii), $u \in V(C_{a-2})$. Note that $x_{a-3} u$ and $u v_n$ are arcs in $T_{C_{a-2}}$ and T_{C_a}, respectively. $x_0 \cdots, x_{a-3} u x_a \cdots x_k$ is an admissible dipath in $G^d_{\mathscr{F}_0}$ and is shorter than Q_0. This contradicts the choice of Q_0.

(V) By (III) and (IV)(ii), $(G_a, \mathscr{P}_a)$ must have some non-trivial vertex and $a \geqslant 3$. Thus, $d_{G_a}(v_0) = 2$.

(VI) By Lemma 6.6, $(G_a, \mathscr{P}_a)$ has a special compatible cycle decomposition $\mathscr{F}_a = \{C'_1, C'_2, ...\}$ such that $v_0 v_1 \in E(C'_1)$ and

Case 1 ($\diamond$). $v_n = x_a$ and some non-trivial vertex v_ℓ of $(G_a, \mathscr{P}_a)$ are both contained in some cycle C'_i with $i \geqslant 2$.

Case 2 ($\diamond\diamond$). Some non-trivial vertex z of $(G_a, \mathscr{P}_a)$ is not contained in C'_1.

Let $\mathscr{F}' = [\mathscr{F}_0 \backslash \{C_{a-1}, C_a\}] \cup \mathscr{F}_a$ which is a special compatible cycle decomposition of $(G, \mathscr{P}')$ and C'_1 is the new bad circuit replacing C_a and all other elements of $\mathscr{F}_a$ are good cycles. By ($\bigstar$), the segments $x_a \cdots x_k$ and $x_0 \cdots x_{a-2}$ of Q_0 remain as dipaths in $G^d_{\mathscr{F}'}$.

In Case 1, the non-trivial vertex v_ℓ in $(G_a, \mathscr{P}_a)$ is also non-trivial in $(G, \mathscr{P})$. By (IV)(ii), $v_\ell \in V(C_{a-2})$. Thus, $x_0 \cdots x_{a-3} v_\ell x_a \cdots x_k$ is an admissible dipath in $G^d_{\mathscr{F}'}$ shorter than Q_0. This contradicts the choice of Q_0.

In Case 2, the bad circuit C'_1 does not contain a non-trivial vertex z of $(G, \mathscr{P})$, this contradicts Lemma 6.4 (1). The proof is completed. ▮

A Technical Lemma

LEMMA 6.6. *Let G_a be an eulerian graph and $\mathscr{P}_a$ be a forbidden system of G_a. Let $\{C_a, C_{a-1}\}$ be a compatible cycle decomposition of $(G_a, \mathscr{P}_a)$ such that*

(a) *$C_a = v_0 \cdots v_s$ is a circuit with $v_s = v_0$ and there are two integers m and n that $0 < m < n < s$ and $d(v_i) = 2$ for each $0 \leqslant i < m$, $d(v_m) = 4$ and $d(v_n) = 2$;*

(b) *C_{a-1} is a connected cycle;*

(c) *$(G_a, \mathscr{P}_a)$ has some non-trivial vertex, and every non-trivial vertex is contained in $\{v_{n+1}, ..., v_{s-1}\}$ and is of degree four.*

Then $(G_a, \mathscr{P}_a)$ has another special compatible cycle decomposition $\{C'_1, C'_2, ...\}$ such that

(1) *each C'_i is connected, C'_1 is a circuit and contains the edge $v_0 v_1$;*

(2) *either*

($\diamond$) *v_n and some non-trivial vertex v_ℓ are both contained in some cycle C'_i with $i \geqslant 2$; or*

($\diamond\diamond$) *some non-trivial vertex is not contained in C'_1.*

Unlike Theorem 6.5, Lemma 6.6 is not a minor-closed result. Hence, by taking the advantage of this, we apply the vertex splitting method in the proof.

For the sake of convenience in the proof, we use the notation

$$V_h = \{v \in V(G_a) : d(v) = h\}, \qquad V_{\geqslant h} = \{v \in V(G_a) : d(v) \geqslant h\},$$

and

$$V^t = \{v \in V(G_a) : v \text{ is trivial}\}, \qquad V^{nt} = \{v \in V(G_a) : v \text{ is non-trivial}\}.$$

Proof of Lemma 6.6. Let $(G_a, \mathscr{P}_a)$ be a counterexample to the lemma with $\sum_{v \in V_{\geqslant 4}} d(v)$ as small as possible.

(I) *The structure of* $(G_a, \mathscr{P}_a)$.

Let $v \in V_2 \backslash \{v_0, v_n\}$ with $E(v) = \{e, e'\}$. Every circuit of G_a containing one of $\{e, e'\}$ must contain both of e, e'. Thus, we always can replace e and e' with a single edge and delete the vertex v. Therefore, we assume that $V_2 = \{v_0, v_n\}$.

We claim that $V_{\geqslant 4} \cap V^t = \{v_m\}$. Assume that $v \in [V_{\geqslant 4} \cap V^t] \backslash \{v_m\}$. We construct a new graph G' from G_a by splitting two edges of C_{a-1} away from the vertex v and preserving C_{a-1} as a connected circle. For the same forbidden system $\mathscr{P}_a$ on G', by our choice of $(G_a, \mathscr{P}_a)$, we have a compatible cycle decomposition of $(G', \mathscr{P}_a)$ satisfying the lemma. Thus, by identifying the pair of split vertices to v, we obtain a compatible cycle decomposition of $(G_a, \mathscr{P}_a)$ satisfying the lemma. This contradicts that $(G_a, \mathscr{P}_a)$ is a counterexample and proves our claim.

So,

$$m = 1, \ n = 2,$$

$$V_2 = \{v_0, v_2\},$$

$$V^t \cap V_{\geqslant 4} = \{v_1\}$$

(that is, v_1 is the only degree four, trivial vertex of $(G_a, \mathscr{P}_a)$),

$$V^{nt} = \{v_3, ..., v_{s-1}\} \neq \varnothing,$$

$$V_{\geqslant 4} = V_4 = V^{nt} \cup (V_{\geqslant 4} \cap V^t) = V^{nt} \cup \{v_1\}$$

(that is, the maximum degree of G_a is 4 since each non-trivial vertex is of degree 4), and C_{a-1} is also a circuit since $V_{\geqslant 4} \cap V^t = \{v_1\}$ which is contained in both C_a and C_{a-1} (Fig. 2). The circuit C_{a-1} is of length at least two since $V(C_{a-1}) = V_4$ and $|V_4| \geqslant 2$. Furthermore, G_a has no loop since both C_a and C_{a-1} are circuits.

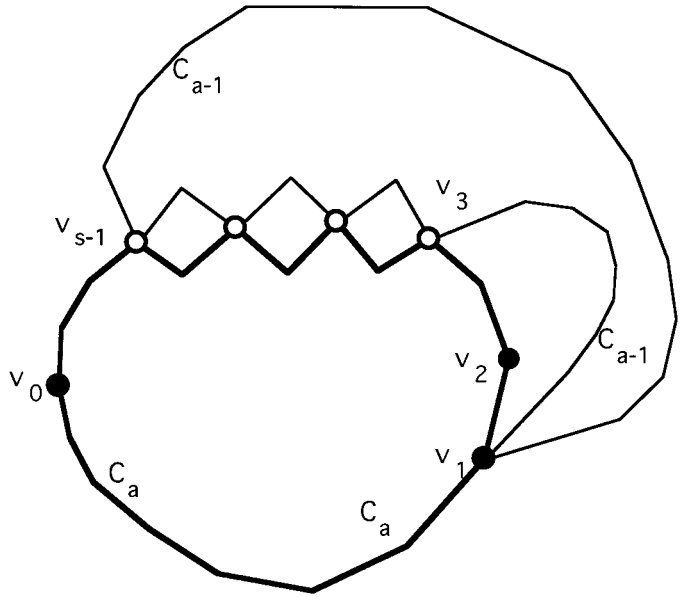

FIG. 2. $(G_a, \mathscr{P}_a)$.

(II) We claim that *for each CCD* $\mathscr{F}'$ *of* $(G_a, \mathscr{P}_a)$, *an element* $D \in \mathscr{F}'$ *containing one of* $\{v_0, v_2\}$ *must contain both.* Assume that $D \in \mathscr{F}'$ contains only v_2 but not v_0. Since $d(v_2) = 2$, we must have that $v_1, v_3 \in V(D)$. Note that $v_3 \in V^{nt}$. Thus, the conclusion $(\diamond)$ of the lemma holds. This contradicts that $(G_a, \mathscr{P}_a)$ is a counterexample.

(III) We claim that *a circuit of* $SP(G_a, \mathscr{P}_a)$ *containing one of* $\{v_0, v_2\}$ *must contain both of them.* Assume that R is a circuit of $SP(G_a, \mathscr{P}_a)$ containing v_2 but not v_0. Then, by Lemma 2.5, $\{C_a \triangle R, C_{a-1} \triangle R\}$ is a compatible cycle decomposition of $(G_a, \mathscr{P}_a)$. It is easy to see that $C_{a-1} \triangle R$ contains v_2 but not v_0. Let $\mathscr{D}$ be the union of circuit decompositions of $C_a \triangle R$, $C_{a-1} \triangle R$. Then $\mathscr{D}$ has an element containing v_2 but not v_0. This contradicts (II) and proves our claim.

(IV) *The structure of the split* $SP(G_a, \mathscr{P}_a)$ *of* $(G_a, \mathscr{P}_a)$. Note that all vertices of $SP(G_a, \mathscr{P}_a)$ are of degree two except for v_1 which is of degree four. The component of $SP(G_a, \mathscr{P}_a)$ containing the vertex v_1 is the union of two circuits, say R' and R'', that $R' \cap R'' = \{v_1\}$. By (III), without loss of generality, let the circuit R' contain the vertices v_0 and v_2 (therefore, contain the segment $v_{s-1}v_0v_1v_2v_3$ of C_a).

(V) By Lemma 2.5, $\{C_a \triangle R', C_{a-1} \triangle R'\}$ is a compatible cycle decomposition of $(G_a, \mathscr{P}_a)$. Let $\mathscr{D}' = \{D_1, ..., D_t\}$ be the union of circuit decompositions of $C_a \triangle R'$ and $C_{a-1} \triangle R'$. Since $C_{a-1} \triangle R'$ contains all

four edges incident with v_1, any circuit decomposition of $C_{a-1} \triangle R'$ must have at least two elements. By Lemma 2.5 again, $C_a \triangle R'$ is not empty. Thus, $t \geqslant 3$. By (II), let D_1 be the circuit containing the segment $v_{s-1}v_0v_1v_2v_3$ of C_a (D_1 is the circuit C_1' described in the lemma). Let D_2 be another circuit containing v_1 since $d(v_1) = 4$. In the rest part of the proof, we are to find a non-trivial vertex contained in D_2 but not in D_1. This would satisfy the conclusion ($\diamond\diamond$) of the lemma and leads to a contradiction.

(VI) We claim that $V(D_2) \cap V(D_1) = \{v_1\}$. If not, assume that $V(D_2) \cap V(D_1)$ contains another degree 4 vertex other than v_1, which must be nontrivial. Let H be the subgraph of G_a induced by edges contained in D_1 and D_2. It is easy to see that $(H, \mathscr{P}_a \mid H)$ also meets all descriptions of the lemma. Since $t \geqslant 3$, H has fewer degree 4 vertices than that of G_a. By our choice of $(G_a, \mathscr{P}_a)$, let $\mathscr{D}''$ be a CCD of $(H, \mathscr{P}_a \mid H)$ satisfying the lemma. Thus, $\mathscr{D}'' \cup \{D_3, ..., D_t\}$ is a CCD of $(G_a, \mathscr{P}_a)$ satisfying the lemma. A contradiction.

(VII) Since G_a has no loop and D_1 contains all vertices of V_2, D_2 must contain two vertices of V_4, one of which, say v, is not v_1 and is not trivial. By (VI), $v \notin V(D_1)$. This meets the conclusion ($\diamond\diamond$) of the lemma and therefore contradicts the assumption that $(G_a, \mathscr{P}_a)$ is a counterexample and completes the proof of the lemma. ▮

7. FAITHFUL CYCLE COVERS

Let H (and H') be a graph with an admissible eulerian weight w (and w'). By $(H', w') \prec (H, w)$, we mean that H' is a subgraph of H and $w'(e) \leqslant w(e)$ for all $e \in E(H')$. (H, w) is called a *contra-pair* if it has no faithful circuit cover. The proof of the circuit cover theorem by Alspach, Goddyn, and Zhang [2] consists of two major parts, one of which is the following result. We give a proof here as an application of Theorem 6.5 and also as a different approach to the circuit cover theorem.

COROLLARY 7.1 (Lemma 1 of [2]). *If (H, w) is a contra-pair, then there exists a contra-pair $(H', w') \preccurlyeq (H, w)$ such that $w'(e) \leqslant 2$ for all $e \in E(H')$.*

Proof. Let $(G, \mathscr{P})$ be obtained from (H, w) by the operation described in Section 1. By Theorem 6.5, there is a minimal contra-pair $(G', \mathscr{P}') \preccurlyeq (G, \mathscr{P})$ such that $|P| \leqslant 2$ for all $P \in \mathscr{P}'$ and $d(v) \leqslant 4$ for all $v \in V(G')$. By the minimality of $(G', \mathscr{P}')$, no pair of vertices is joined by more than two parallel edges in G'. Therefore, $(G', \mathscr{P}')$ gives rise to a contra-pair $(H', w') \preccurlyeq (H, w)$ with the required property. ▮

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